



Contribution ID: 16

Type: poster

Spin Wave Normalization Towards all Magnonic Circuits

The key enabling factor for Spin Wave (SW) technology utilization for building ultra-low power circuits is the ability to energy efficiently cascade SW basic computation blocks. SW Majority gates, which constitute a universal gate set for this paradigm, operating on phase encoded data are not input output coherent in terms of SW amplitude. Thus, their cascading requires information representation conversion from SW to voltage and back, which is by no means energy effective. In this paper, a novel conversion free SW gate cascading scheme is proposed that achieves SW amplitude normalization by means of a directional coupler. After introducing the normalization concept, we utilize it in the implementation of three simple circuits and, to demonstrate its bigger scale potential, of a 2-bit inputs SW multiplier. The proposed structures are validated by means of the Object Oriented Micromagnetic Framework (OOMMF) and GPU-accelerated Micromagnetics (MuMax3). Furthermore, we assess the normalization induced energy overhead and demonstrate that the proposed approach consumes 1.25x to 1.5x less energy when compared with the transducers based conventional counterpart. Finally, we introduce a normalization based SW 2-bit inputs multiplier design and compare it with functionally equivalent SW transducer based and 16nm CMOS designs. Our evaluation indicates that the proposed approach provided 1.34x and 6.25x energy reductions when compared with the conventional approach and 16nm CMOS counterpart, respectively, which demonstrates that our proposal is energy effective and opens the road towards the full utilization of the SW paradigm potential and the development of SW only circuits.

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Session Classification: Posters

Track Classification: Spins and spin waves