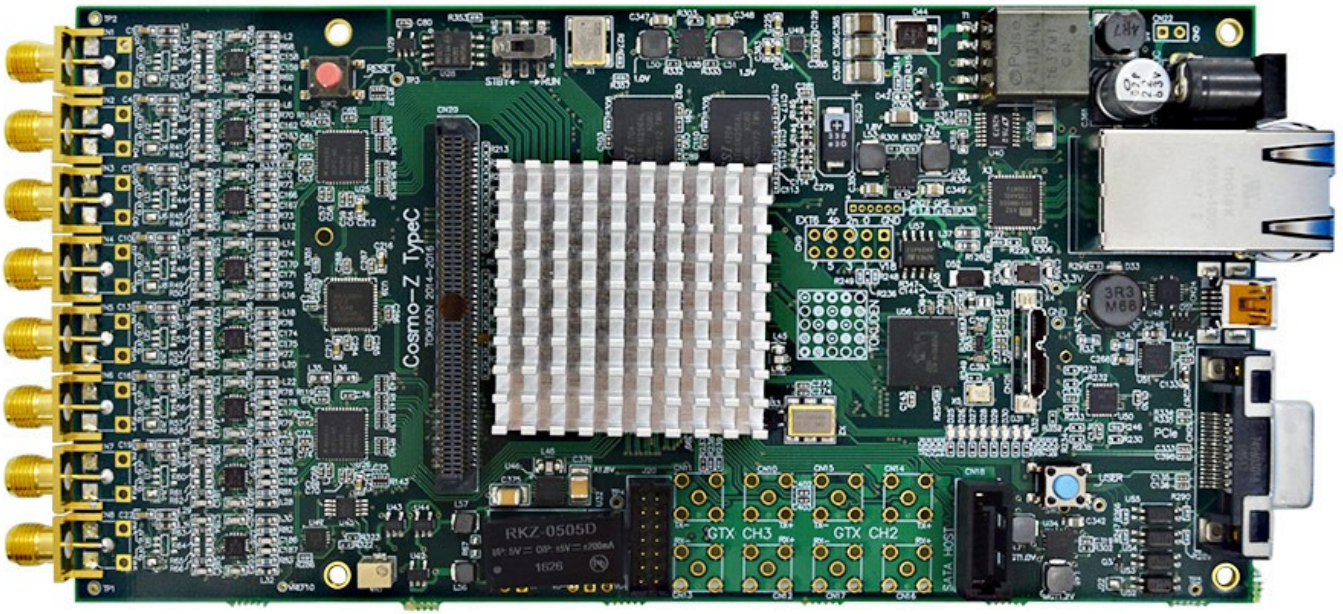
FAST data acquisition at Cosmo-Z board

Jiří Záhora

- 8 channels of 12-bit 125MHz ADC
- XILINX's FPGA "ZYNQ"



Why FPGA

- Field-programmable gate array
- It’s fast
- Signal processing during acquisition
- Reducing amount of data

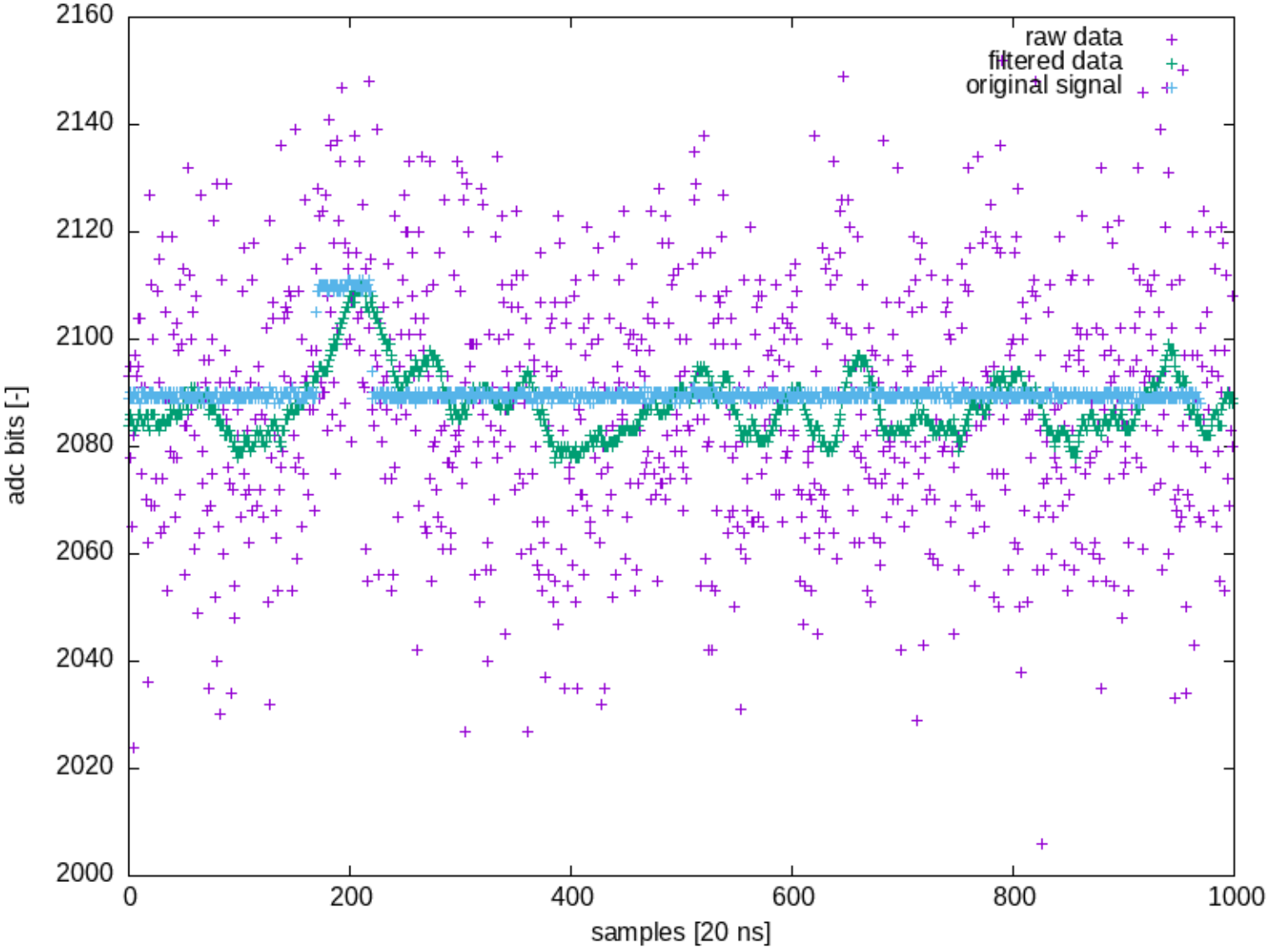
Math restrictions for HW implementation

- Easy operations
  - add, substract, multiply, divide 2^n
- Difficult operations
  - general division, square root

Trigger condition: $\frac{\mathrm{fir}(sig) - \mathrm{mean}(nsb)}{\mathrm{stdev}(nsb)} > threshold$

Rewrite for FPGA implementation:

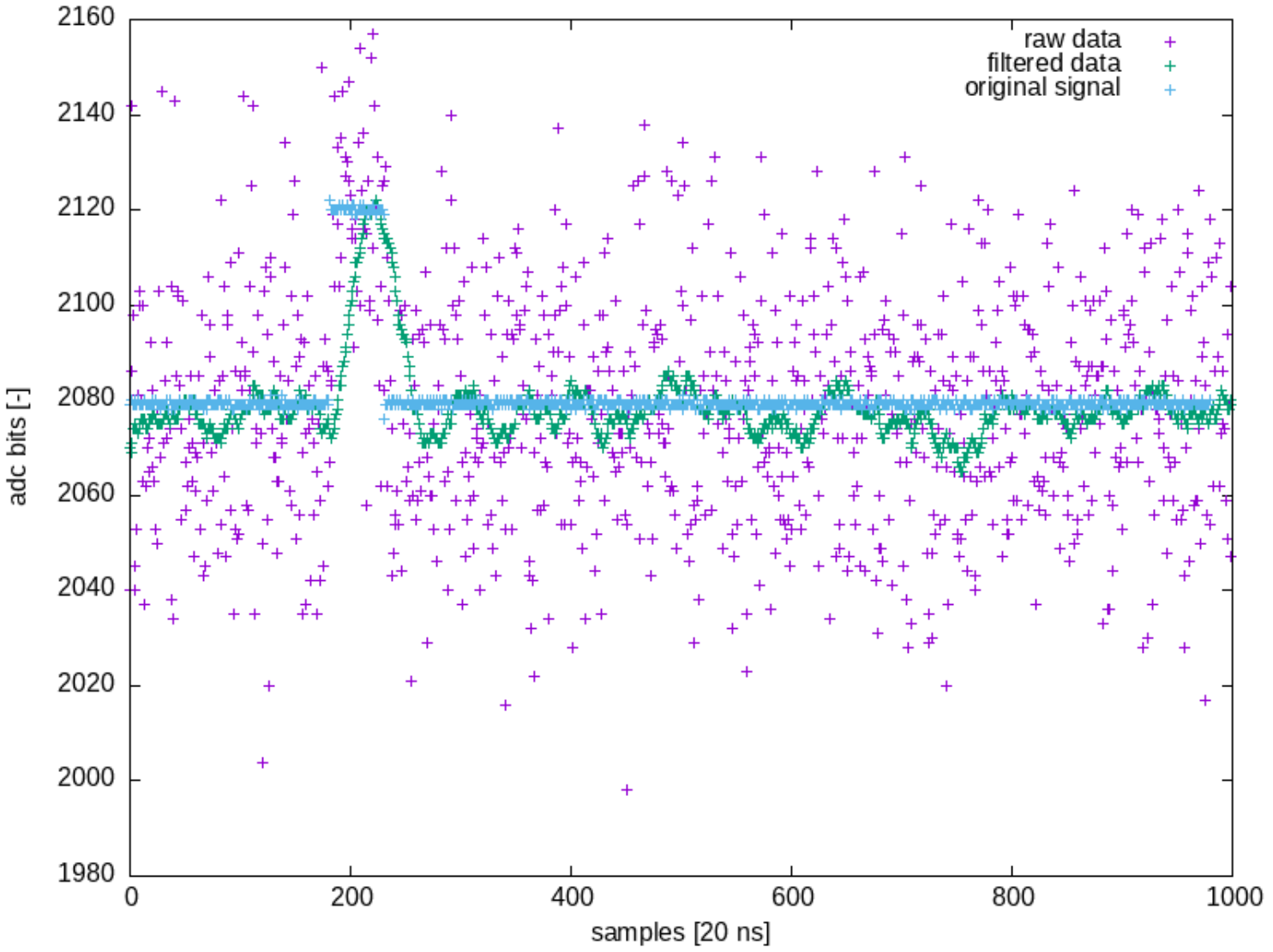
$$(\mathrm{fir}(sig) - \mathrm{mean}(nsb))^2 > threshold \cdot \mathrm{var}(nsb)$$

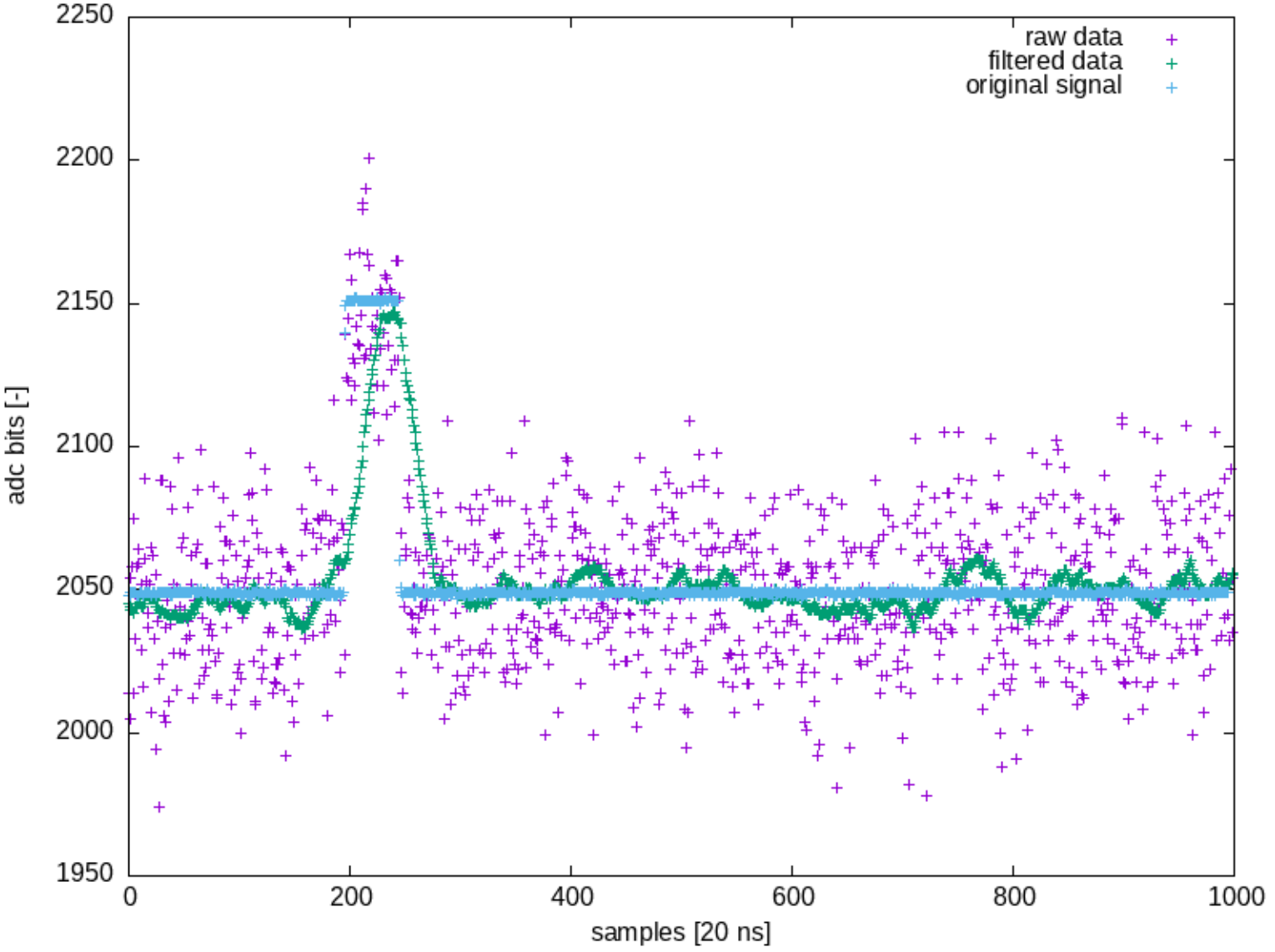

raw data
filtered data
original signal
adc bits [-]
samples [20 ns]
2160
2140
2120
2100
2080
2060
2040
2020
2000
0
200
400
600
800
1000

Next steps

- Better signal filtering
  - Currently moving average filter (width = 64)
  - Implement FIR filter, different widths, thresholds
- Rewrite code for better parametrization
- Add GPS timestamps
- Repair broken board

Thanks for attention


raw data
filtered data
original signal
adc bits [-]
samples [20 ns]
2160
2140
2120
2100
2080
2060
2040
2020
2000
1980
0
200
400
600
800
1000


raw data
filtered data
original signal
adc bits [-]
samples [20 ns]
2250
2200
2150
2100
2050
2000
1950
0
200
400
600
800
1000